

Phase-Locked Loops : Design, Simulation, And Applications (Professional Engineering) By Roland E. Best

By Roland E. Best

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a phase-locked loop (PLL) is designed to lock the phase of an , we will first design the PLL in the for the simulation, including the carrier phase and <http://liquidsdr.org/blog/pll-howto/>

Applications . Phase-locked loops are widely To keep phase noise low in PLL circuits, it is best to avoid R. E. (2003), Phase-locked Loops: Design, http://en.wikipedia.org/wiki/Phase-locked_loop

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Behavioral modeling phase-locked loops for mixed Best, Phase-Locked Loops: Theory, Design and of an analog charge-pump phase locked loop .Simulation 50,
<http://link.springer.com/article/10.1007/BF00713978>

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CSE 577 Spring 2011 Phase Locked Loop Design KyoungTae Kang, Kyusun Choi Electrical Engineering Computer Science and Engineering Computer Science and Engineering
<http://www.cse.psu.edu/~kxc104/class/cse577/11s/lec/S09PLL.pdf>

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Apr 24, 2015 In this introductory video tutorial I simulate a phase locked loop (PLL) using NI AWR Visual System Simulator (VSS). The goal of these "virtual experiments"
<http://www.youtube.com/watch?v=JiBF2ZGhPpI>

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